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MIRI-PD
Processor Design
2019-2020 Student Projects Overview

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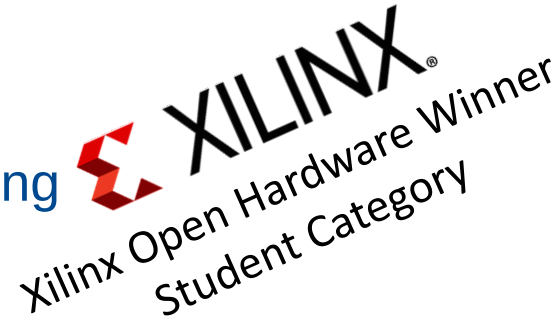
14/09/2021

RISC-V Educator of the Year Award 2019

- 7 projects based on RISC-V
  - 2 BSC's Lagarto
    - Core improvements, vector extensions
  - 3 Western Digital SweRV
    - Measurement-Based Probabilistic Timing Analysis (MBPTA) compliance, dual and triple lock step designs
  - 1 Ariane
    - ECC
  - 1 Rocket
    - Cryptographic Accelerator
- 5 CPU projects
- 2 accelerators

Fall 2020 Projects

- 8 projects in total, 5 based on RISC-V
  - BSC's Lagarto
    - Out-of-order execution, integration with vector accelerator
  - Western Digital SweRV
    - Measurement-Based Probabilistic Timing Analysis (MBPTA) compliance on EH2
  - LEON 3 and NOEL-V
    - Short vector unit for machine learning
  - MIPS
    - Time predictable multithreading



Fall 2020 Projects

- 8 projects in total, 5 based on RISC-V
  - Vortex GPU
    - Time predictability and reliability
  - Custom GPU
  - Binary Neural Network accelerator for space processors
  - TPU-like accelerator

Xilinx Open Hardware Competition 2020

- 8 projects in total, 5 based on RISC-V
  - Vortex GPU
    - Time predictability and reliability
  - Cu
  - Bir
  - TP

What all these projects have in common?

Common Projects Theme





- Improvements to existing RISC-V processors focusing on features for critical and real-time systems
- These features have not received much attention from the RISC-V community yet

Critical and Embedded Systems 1/3

- Dual and triple lockstep processors:
  - Reliability feature useful for aerospace, avionics and nuclear reactor applications (triple lockstep) or automotive (dual-lockstep).
- Time-predictable cores and Measurement-Based Probabilistic Timing Analysis (MBPTA)-compliant cores and GPUs featuring a random-placement cache [1] and fixed-latency instructions
  - useful for all critical domains e.g. aerospace, avionics and automotive applications, which require computation of Worst Case Execution Time (WCET).

[1] L. Kosmidis et al. A cache design for probabilistically analysable real-time systems. DATE 2013

Critical and Embedded Systems 2/3

- ECC protection
  - Reliability feature useful for all critical domains e.g. aerospace, avionics and automotive applications.
- Vector accelerator unit
  - Features useful for all critical domains e.g. aerospace, avionics and automotive applications, which require high-performance, e.g. for autonomous operation.
- Cryptographic accelerator
  - Feature useful for all critical domains, which require strong security and privacy in connected environments e.g. medical, automotive, nuclear plants.

Critical and Embedded Systems 3/3

- Machine Learning accelerators
  - Useful for all critical domains, which require machine learning environments e.g. automotive, avionics, aerospace, medical etc

Who is interested in Safety Critical and Real-time Systems?

- European Space Agency (ESA)
- Airbus
- Automotive companies

- 3 projects related to these industries are on going at BSC

Follow-up/Parallel Activities

- Master Theses building on the developed projects
  - Performance evaluation, extensions
- Potential Publication(s)
- Xilinx Open Hardware Contest (http://www.openhw.eu)
  - Registration in February, projects submitted by end of June
  - 1500 € prize
- Hack@DAC: Hw Security Competition (https://hackatevent.org/hackdac21/)
  - October 4, Registration end and phase 1 start
  - November 19, phase 1 finishes
  - Phase 2, at the Design Automation Conference (DAC) in San Francisco
  - Monetary prize for students
- Both offered as a SIRI Seminars for additional ECTS

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